IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	10/665,654	Confirmation No. 8565
Applicant	:	David Jia Chen et al.	
Filed	:	09/18/2003	
TC/A.U.	:	2816	
Examiner	:	Linh M. Nguyen	
Docket No.	:	ROC920030233US1	
Customer No.	:	23334	

PRE-APPEAL BRIEF REQUEST FOR REVIEW

The following remarks are submitted with the Applicants' notice of appeal. The references cited by the Examiner do not teach each and every element in the independent claims of the instant application, as required by 35 U.S.C. § 102.[1]

Electronic circuit designs typically include arrangements for synchronizing operations of digital circuits. It is common to provide one or more clocks for control of the timing operation of most digital circuits. However, a complicating factor in the design of digital circuits is that clock signals are subject to propagation delays and other forms of distortion as they are distributed to various elements of a digital circuit. Typically, electronic delay elements are used on integrated circuits to adjust path timing or to generate extended pulses used for clocking imbedded arrays.

Elements that can generate extended delays are not only difficult to design but are also difficult to fabricate. One traditional delay element comprises a series of inverter gates. These inverter gates configurations used significantly more space (approximately four times) and more power than the conventional type of delay elements.

Also, prior art delay elements use various channel length devices which create problems in the modeling and processing of integrated circuits. Typically in production,

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[1] See MPEP §2131 (Emphasis Added) "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim."

the process is "tuned" to be optimal for a given channel length. Consequently, this results in variations of channels that are outside the "tuned range." The process in the prior art cannot be tuned to accommodate these high degrees of variation.

Across chip length variation (ACLV) typically is a fixed number in a production process. For example, an 80-nanometer channel length with a tolerance of 10-nanometer yields a 10/80 (12.5%) variation across chips. Compare this to an extended channel length of 280 nanometers, which provides a tolerance of 10/280 or 3.6%. This mixture of channel lengths results in non-uniform tolerance variations across the circuit. Accordingly, the tolerances across the delay stages will not properly track the tolerances of other circuits on the chips. This is especially a problem with timing elements, since delays through delay circuits with extended channel lengths will vary across the chip by a different amount than other minimum channel length circuits.

The present invention, on the other hand, overcomes the problems discussed above with the prior art by providing a delay element for use in integrated circuits. Each of the delay stages in the delay element includes a stack of uniform channel length transistors. Unlike conventional delay elements, the present invention does not use extended channel length transistors. The uniform channel length transistors allow the tolerances across the delay stages to track tolerance of other circuits on a chip. In other words, the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip.

Sato Does Not Teach Uniform Channel Length Transistors

Independent claims 1 and 9-11 each recite "wherein each of the delay stages includes a stack of uniform channel length transistors". Clearly this is not taught by Sato. Independent claims 1 and 9-11 further recite "without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other circuits on a chip". Clearly this is also not taught by Sato.

Furthermore, independent claims 1 and 9-11 recite "the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip". Clearly this is also not taught by Sato. Accordingly, independent claims 1 and 9-11 distinguish over Sato for at least these reasons and the Examiner's rejection should be withdrawn.

The Sato reference cited by the Examiner discloses a synchronous semiconductor memory device that is operable in a snooze mode. See Sato Abstract and col. 2, lines 61-67 to col. 3, lines 1-17. The Examiner directs Applicants to FIG. 14A and col. 14, lines 35-26 of Sato, wherein Sato discloses that the "[g]ate circuits 60a-60n have the same structure". This is the only support that the Examiner gives for rejecting the claim element of "wherein each of the delay stages includes a stack of uniform channel length transistors". Sato teaches that the gate circuits have the same structure, which is not the same as the transistors within the gate circuits being of uniform channel length. The disclosure of "[g]ate circuits 60a-60n have the same structure" should be interpreted as each gate circuit having the same number of transistors, the same type of transistors, etc. as show in FIG. 14A of Sato. In fact, Sato is completely silent on the transistors being of uniform channel length. Careful reading of Sato does not teach or suggest that the transistors P1-P3 and N1-N3 are uniform channel length transistors. Accordingly, independent claims 1 and 9-11, distinguish over Sato for at least these reasons as well and the Examiner's rejection should be withdrawn.

Moreover, the Examiner failed to point out where Sato teaches that the delay element includes uniform channel resistors "so that tolerances across the delay stages track tolerance of other circuits on a chip" and that "the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip". As stated above, the Examiner asserts that Sato teaches the gate circuits having the same structure and, therefore, the Examiner concluded Sato teaches these two claim elements.

Sato is directed towards the post-production stage of the circuit and is not concerned with providing uniform tolerance variations a circuit across a circuit during production. A post-production stage such as manufacturing/yield is not the same as parametric tracking. Yield is one measurement among several of the efficiency in a chip manufacturing process. Manufacturing yield is a reflection of the quality of the manufacturing process and drives cost. The present invention, on the other hand, is concerned with the manufacturing process, which naturally varies from wafer to wafer, by using parametric tracking. Designs that use a mixture of channel lengths result in non-uniform tolerance variations across the chip. In contrast the present invention eliminates this problem "without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other circuits on a chip; wherein the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip."

In view of the foregoing, independent claims 1 and 9-11 distinguish over Sato because one or more claim elements are not present in Sato. All the remaining claims i.e. 2-10, and 13-14 depend respectively from independent claims 1 and 9-11. Accordingly, the claims 1-14 of the present invention distinguish over Sato for the reasons shown above. The Applicant respectfully request that the claims 1-14 of the present invention be allowed or in the alternative reopen prosecution on the merits citing art teaching every element recited in the claims.

Respectfully submitted,

Date: January 17, 2006

By: _____
Jon Gibbons, Reg. No. 37,333
Attorney for Applicants

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Docket Number (Optional)
ROC920030233US1

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on January 17, 2006

Signature Karen Tarageweski

Typed or printed name Karen Tarageweski

Application Number	Filed
10/665,654	9/18/03

First Named Inventor: David Jia Chen

Art Unit	Examiner
2816	Linh M. Nguyen

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

☑ attorney or agent of record.
Registration number 37,333

☐ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____

Signature

Jon A. Gibbons
Typed or printed name

(561) 989-9811
Telephone number

1/17/06
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required.
Submit multiple forms if more than one signature is required, see below*.

☑ *Total of 1 forms are submitted.